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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,119	03/19/2004	Hongzhong Xu	001.3004 (SC12973ZC)	8493

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EXAMINER	
DANG, ROBERT TRONG	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,119	XU ET AL.	
	Examiner	Art Unit	
	Robert T. Dang	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: There no description to what the "fifth region" is in the specification.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-14 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by applicants own acknowledge prior art (APA).

As to claim 1, APA discloses in figure 1, an electrostatic discharge (ESD) protection device having a first terminal (15) and a second terminal (20), the device comprising: a transistor (25) having a collector coupled to the first terminal (15) of the ESD protection circuit, a base and an emitter coupled to the second terminal (20) of the ESD protection circuit; and a zener diode (30) having a first terminal coupled to said collector of said transistor (25) and a second terminal coupled said base of said vertical transistor (25) wherein said zener diode breaks down in an ESD event providing impact ionization current to a base region of said transistor and wherein subsurface current paths are provided in said base region to redistribute current away from a surface of said base region to increase a peak current handled by the ESD protection device (see page 4, paragraph [0012] of the specification).

As to claims 2-4, APA discloses in figure 2, a substrate (105) of a first type; an epitaxial layer (110) of a second type; and an isolation region (120) of a first type (p-type) formed in said epitaxial layer for defining an active area of the ESD protection device, said active area corresponding to said epitaxial layer interior to said isolation region (see page 2, paragraph [0008] of the specification). Applicant also discloses that an isolation region comprising a deep trench is well known in the art (see page 7, paragraph [0028] of the specification).

As to claims 5, APA discloses in figure 2, a base region (130) of said first type formed in said active area; an emitter region (145) of said second type (n-type) formed in said base region (130), said emitter region (145) coupling to the second terminal (20) of the ESD protection device; a first region (140_1) of said first type (p-type) formed in

said base region (130), said first region being spaced a predetermined distance from said emitter region; and a second region (140_2) of said first type (p-type) formed in said first region, said second region coupling to the second terminal (20) of the ESD protection device wherein a depth of said first region into said base region is greater than a depth of said second region (see page 3, paragraphs [0009-0010] of the specification).

As to claims 6, APA discloses in figure 2, wherein said doping concentration of said second region is greater than a doping concentration of said first region (see page 3, paragraph [0011] of the specification).

As to claims 7, APA discloses in figure 2, wherein said first region (125) is formed in a ring shape and wherein said emitter region is centrally located interior to said ring shape of said first region and wherein a depth of said first region in said base region is greater than a depth of said emitter region (see page 3, paragraph [0009] of the specification).

As to claim 8, APA discloses in figure 2, a buried layer of said second type underlying a portion of said active area; and a third region (125) of said second type spaced a predetermined distance from said base region, said third region coupling to said buried layer and the first terminal of the ESD protection device (see page 3, paragraph [0010] of the specification).

As to claim 9, APA discloses in figure 2, wherein said third region (125) is formed in a ring shape and wherein said base region (130) is located interior to said ring shape of said third region (see page 3, paragraph [0010] of the specification).

As to claim 10, APA discloses in figure 2, further including a fourth region (150) of said first type formed overlying a boundary between said base region and said epitaxial layer (see page 3, paragraph [0011] of the specification).

As to claim 11, APA discloses in figure 2, wherein said zener diode comprises said fourth region (150), said epitaxial layer (110), and said third region (125) (see page 3, paragraph [0011] of the specification).

As to claim 12, APA discloses in figure 2, a method of protecting a semiconductor device from an electrostatic discharge comprising the steps of: breaking down a zener diode during an electrostatic discharge (ESD) event such that an impact ionization current is generated; and enabling a transistor with said impact ionization current to dissipate said ESD event before the semiconductor device is damaged wherein said impact ionization current is distributed uniformly through a base region of said transistor to prevent current crowding at a surface of said base region (see page 3, paragraph [0012] of the specification).

As to claim 13, APA discloses in figure 2, further including a step of distributing said ionization current below a surface of said transistor (see page 3, paragraph [0012] of the specification).

As to claim 14, APA discloses in figure 2, further including a step of reducing a resistance in a path of said impact ionization current (see page 3, paragraph [0012] of the specification).

As to claim 17, APA discloses in figure 2, a buried layer (115) underlying said base region (130); a third region (125) of said second type formed in said epitaxial layer

(110) interior to said isolation region, said third region extending from a surface of said epitaxial layer to said buried layer; and a fourth region (135) of said second type formed in said third region (125), said fourth region coupling to the first terminal (15) of the ESD device current (see page 3, paragraphs [0010-0011] of the specification).

Claim Rejections - 35 USC § 103

2. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicants own acknowledge prior art (APA) in view of Ralign (6365462).

As to claim 15, APA discloses in figure 2, a substrate (105) of a first type; an epitaxial layer (110) of a second type; and an isolation region of a first type (120) formed in said epitaxial layer for defining an active area of the ESD protection device, said active area corresponding to said epitaxial layer interior to said isolation region (see page 2, paragraph [0008] of the specification); a base region (130) of said first type formed in said active area; an emitter region (145) of said second type formed in said base region, said emitter region coupling to the second terminal of the ESD protection device; a first region of said first type formed in said base region adjacent to said emitter region wherein said first region has a depth greater than a depth of said base region and wherein said first region is coupled to said emitter region; and a zener diode having a first terminal coupled to said epitaxial layer interior to said isolation region and a second terminal coupled to said base region. (see page 3, paragraphs [0009-0011] of the specification). However, the reference does not disclose the depth of the first region

being greater than 30% of the depth of the base region. Ralign discloses in his an invention wherein the depth of the first region of the first type being greater than 30% of the depth of the base region (see col. 15, lines 13-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device and make depth of the first region of the first type being greater than 30% of the depth of the base region to ensure good contact.

Also, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233*

As to claim 16, APA discloses in figure 2, including a second region of said first type formed in said first region of said first type wherein said first region has a higher doping concentration than said base region and wherein said second region has a higher doping concentration than said first region ((see page 3, paragraphs [0009-0011] of the specification).

3. Claims 18-20 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicants own acknowledge prior art (APA) in view of Snyder et al (4367509).

As to claims 18-19, APA discloses in figure 2, all the limitations discussed above including a zener diode (30) comprised of the third (125), epitaxial (110), and isolation (120) regions, but does not disclose the fifth region of said first type overlying a boundary of between said base region and said epitaxial region interior to said isolation region. However, Snyder discloses in his invention an ESD device (fig. 2) including the fifth region of said first type (P-type) overlying a boundary of between said base region

(110) and said epitaxial region (104) interior to said isolation region (see claims 3 and 6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device and add the fifth region with the zener diode encompassing it, in order to conductively couple the emitter portion of the transistor to other elements of said power output circuit located on the integrated circuit chip during normal operating conditions.

As to claim 20, APA discloses in figure 2, wherein the first terminal of the ESD device couples to circuitry of an integrated circuit to be protected and wherein said the second terminal of the ESD device couples to ground (see page 2, paragraph [0004] of the specification).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert T. Dang whose telephone number is 571-272-8326. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl D. Easthom can be reached on 571-272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RTD

KARL EASTHOM
SUPERVISORY PATENT EXAMINER